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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,593	04/19/2000	Ronald J. Gagnon	9-13528-102US	4092

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EXAMINER	
PHILPOTT, JUSTIN M	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/552,593	GAGNON ET AL.	
	Examiner	Art Unit	
	Justin M. Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,16-30,36-44 and 52* is/are rejected.

7)☒ Claim(s) *10-15,31-35 and 45-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 28, 2005 has been entered.

Response to Arguments

2. Applicant's arguments filed June 15, 2005 have been fully considered but they are not persuasive.

3. Specifically, applicant argues (pages 2-4) that Parruck does not teach the output timer as recited in applicant's claims, and particularly, in applicant's claim 1. Further, applicant argues that Parruck does not teach the aligning step as recited in applicant's claim 52. With respect to these arguments, Examiner maintains the position that Parruck does in fact teach such limitations as recited in applicant's claims. The following office action discusses Parruck with more detail in an effort to clarify Examiner's position in response to applicant's arguments. Accordingly, in view of the following office action, applicant's arguments are not persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 4-9, 16-23, 25-30, 36-44 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,257,261 to Parruck et al.

Regarding claims 1, 19-22, 39-41 and 52, Parruck teaches a channel processor (e.g., 10-2 in FIG. 1a) adapted for aligning a respective first data stream (e.g., STS-3#2, also see col. 3, lines 15-23 wherein the data streams may comprise the concatenation of any number of STSn data streams) with a second data stream (e.g., STS-3#1), each data stream being conveyed within a respective parallel channel and having substantially equivalent bit and frame rates (e.g., see col. 3, lines 24-68), the channel processor (e.g., 10-2 in FIG. 1a) being connected to a respective channel for processing the respective first data stream (e.g., STS-3#2), and comprising: a) a framer (e.g., via demultiplexer 40 in FIG. 2) adapted to detect incoming frames and generate a local strobe signal (e.g., comprising J1 byte) indicative of a timing of incoming frames of the respective first data stream (e.g., see col. 7, lines 1-21); b) a memory (e.g., FIFOs 45 in FIG. 2) for buffering incoming bits of the respective first data stream (e.g., see col. 6, lines 48-68); c) an interface (e.g., adjacent terminating apparatus, see col. 5, lines 9-21) adapted to receive a master strobe signal (e.g., comprising control signal and B3 parity value) from a selected adjacent channel processor (e.g., master apparatus, see col. 5, lines 9-21); and d) an output timer (e.g., see retiming block 18 in FIG. 1d) adapted to control a position of a read pointer (e.g., via pointer recalculation, see FIG. 1d and col. 5, line 35 – col. 7, line 21) for outgoing bits of the respective

first data stream (e.g., STS-3#2) based on a selected one of the local (e.g., comprising J1 byte) and master (e.g., comprising control signal and B3 parity value) strobe signals (e.g., see col. 5, line 66 – col. 6, line 47).

Further, regarding claims 20-22 and 39-41, Parruck teaches a control unit adapted to: a) designate a master channel processor (e.g., master 10-1, see FIGS. 1a and 1b and col. 3, lines 46-49) to operate in a free-running mode in which the timing of outgoing bits of a respective master hyper-concatenated data stream is based on the respective local strobe signal (e.g., see col. 4, lines 1-68); and b) designate a slave channel processor (e.g., 10-2, see col. 3, lines 46-49) to operate in a slave mode in which the timing of outgoing bits if a respective slave hyper-concatenated data stream is synchronized to that of the master data stream based on a master strobe signal (e.g., comprising control signals, see col. 3, lines 42-68) originating from the master channel processor. Furthermore, Parruck teaches a set of two of more adjacent slave channel processors (e.g., 10-2, 10-3) to successively propagate a strobe signal (e.g., comprising control signals) originating from the master channel processor to each one of the set of adjacent slave channel processors, whereby the timing of outgoing bits of each respective slave data stream is synchronized with that of the master data stream (e.g., see col. 3, lines 42-68).

Further, regarding claim 52, Parruck teaches providing an end-to-end path between a source node and a destination node (e.g., nodes 7 and 8, see FIG. 1a), the end-to-end path comprising as least M parallel channels (e.g., A-D); inverse multiplexing (e.g., via multiplexer/demultiplexer at node 7, see col. 3, lines 24-41) the high bandwidth signal (e.g., STS-12c) across M (e.g., four) data streams (e.g., STS-3#n, wherein n equals 1 to 4, see FIG. 1a); launching each data stream (e.g., STS-3#n) from the source node toward the destination

node (e.g., nodes 7 and 8, see FIG. 1a) through respective ones of the channels (e.g., A-D); aligning (e.g., via demultiplexer/multiplexer embodiment of FIG. 2) each of the data streams at a downstream end (e.g. at node 10-#, see FIGS. 1a, 1d and 2) of each hop toward the destination node (e.g., nodes 7 or 8, see FIG. 1a); and reassembling the high-bandwidth signal (e.g., STS-12c) at the destination node (e.g., at node 7, which outputs STS-12c in FIG. 1a).

Regarding claim 2, Parruck further teaches that the data streams comprise an arbitrary mix of concatenated and non-concatenated SONET signals by disclosing that the signals may include, e.g., STS-3 and STS-3C (e.g., see col. 1, lines 37-43; FIG. 2 and col. 2, lines 62-63; and col. 9, lines 22-23 wherein Parruck discloses STS-3 is used generally to indicate the signal may be either a non-concatenated STS-3 signal or a concatenated STS-3C signal).

Regarding claims 4, 25 and 43, Parruck teaches the framer comprises: a) a detector circuit (e.g., frame counter 50) adapted to generate a detection signal (e.g., frame count) indicative of detection of a selected byte (e.g., H3 byte) of each incoming frame of the respective first data stream; and b) a strobe circuit (e.g., decision block 52) adapted to generate the local strobe signal (e.g., comprising J1 byte at multiplexer 55) with a predetermined timing relative to the detection signal (e.g., see col. 6, line 48 – col. 9, line 23).

Regarding claims 5, 26, and 44, Parruck teaches detecting J1 bytes of incoming SONET frames and generating a detection signal with a predetermined timing relative to the reception of the J1 byte (e.g., see col. 7, lines 1-21). However, Parruck may not specifically disclose detecting one or more of A1 and A2 bytes of incoming SONET frames and generating the detection signal with a predetermined timing relative to reception of the A1 byte. Parruck further teaches, however, that while a particular byte (i.e., J1 byte) is described as being used for

accomplishing realignment, it will be appreciated that different bytes could be utilized (e.g., see col. 14, lines 51-61). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to detect the A1 or A2 bytes instead of J1 bytes in the system of Parruck as suggested by Parruck by teaching that different bytes could be utilized to accomplish the same realignment.

Regarding claims 6 and 27, Parruck teaches the memory is a FIFO buffer (e.g., FIFOs 45, see FIG. 2) having a read pointer (e.g., READ#1) indicative of an address of an outgoing bit of the respective first data stream.

Regarding claims 7 and 28, Parruck teaches a storage capacity of the memory (e.g., FIFOs 45) is selected on a basis of a maximum anticipated misalignment between the first and second data streams (e.g., see col. 7, lines 47-69, wherein the FIFO accommodates up to 12 bytes of delay).

Regarding claims 8, 9, 29 and 30, as discussed above regarding claims 7 and 28, Parruck teaches a storage capacity of the memory (e.g., FIFOs 45) is selected on a basis of a maximum anticipated misalignment between the first and second data streams (e.g., see col. 7, lines 47-69). Furthermore, Parruck teaches the storage capacity of the memory (e.g., twenty-nine bytes deep and ten bits wide) is selected to provide suitable processing. However, Parruck may not specifically disclose the memory is specifically equivalent to the number of bits received during an interval of up to 250 nsec or the size of up to one-half of a data frame. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32

USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the storage capacity of the memory to a size of the number of bits received during an interval of up to 250 nsec or the size of up to one-half of a data frame, since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value.

Regarding claims 16 and 36, Parruck teaches the interface comprises first and second input circuits (e.g., at rxB3 and rxSPE in FIG. 1b, coupled to demultiplexer 40 in FIG. 2) adapted to receive a master strobe signal from a respective one of the first and second adjacent channel processors.

Regarding claims 17 and 37, Parruck teaches a direction selector circuit (e.g., FIG. 2) is adapted to couple (e.g., via multiplexer 50) a selected one of the first and second input circuit to the output timer (e.g., retimed clock output), such that a master strobe signal propagated from a direction of the selected adjacent channel processor can be used by the output timer.

Regarding claims 18 and 38, Parruck teaches the interface further comprises first and second output circuits (e.g., at txB3 and txSPE in FIG. 1b) adapted to send a selected one of the local strobe signal and the master strobe signal to a respective one of the first and second adjacent channel processors.

Regarding claims 23 and 42, Parruck teaches the first and second hyper-concatenated data streams comprise concatenated SONET signals (e.g., see col. 1, lines 63-68).

6. Claims 3 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parruck in view of U.S. Patent No. 6,160,819 to Partridge et al.

Regarding claims 3 and 24, Parruck teaches the system as discussed above regarding claims 1 and 19, however, Parruck may not specifically disclose the parallel channels comprise a wavelength of a WDM optical communications system.

Partridge teaches a method for multiplexing bytes over parallel communication links. Specifically, Partridge discloses it is well known in the art that by transmitting information in parallel the overall capacity on a SONET system can be increased (e.g., see col. 2, lines 30-32). Furthermore, Partridge discloses it is well known in the art that WDM allows for high speed transmission at a lower cost and a higher degree of reliability (e.g., see col. 2, lines 32-37). The invention of Partridge teaches a technique for aggregating multiple high speed links for delivery to other communication points utilizing WDM, wherein lower costs and higher efficiencies are achieved (e.g., see col. 3, line 13 – col. 4, line 4). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Partridge to the system of Parruck in order to achieve lower costs and higher efficiencies.

Allowable Subject Matter

7. Claim 10-15, 31-35 and 45-51 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

claims 10, 11, 31 and 45 recite a processor/system/method as in respective claims 6, 27 and 39, and further comprise: a) phase error detection wherein a phase error is detected between the local strobe signal and the master strobe signal, and b) pointer adjustment wherein the read pointer is adjusted based on the detected phase error; claims 12-15, 32-35 and 46-51 are dependent upon claims 10, 31 and 45, respectively, and include the above as well as further limitations.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M. Philpott whose telephone number is 571.272.3162. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on 571.272.3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin M Philpott

ALPUS H. HSU
PRIMARY EXAMINER